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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,471	01/25/2001	Shinichi Minami	843.39542X00	3956

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EXAMINER
BAUMEISTER, BRADLEY W

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/768,471	Minami et al.
Examiner	**Art Unit**
B. William Baumeister	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *12/23/02 and 1/21/03*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-11, 15-24, 26, 27, and 29-38* is/are pending in the application.

4a) Of the above, claim(s) *4-11, 15-21, and 23* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-3, 22, 24, 26, 27, and 29-38* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☒ The proposed drawing correction filed on *Jan 21, 2003* is: a) ☒ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 1/21/2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Objections

2. Claims 24 and 32-35 are objected to because of the following informalities:

a. Claim 24 (latest version appears in amendment B, paper #11, filed 4/26/2002) still recites that the second semiconductor region has an impurity concentration higher than that of said semiconductor substrate. This is in contradistinction to claims 26 and 27 which were subsequently corrected to recite that the second semiconductor region impurity concentration is higher than that of the well region. A review of the specification and comments associated with Amendment C indicate that claim 24 was intended to also be similarly amended/corrected. As such, the Examiner is provisionally interpreting claim 24 to possess a clerical error intending to read "well region" instead of "semiconductor substrate," but appropriate correction is required to confirm this interpretation. The examiner's interpretation is supported by the fact that the specification as originally filed does not set forth any doping concentrations for the substrate, and

a reading of claim 24 to intend to recite "substrate" might raise 112-1st paragraph new matter issues.

b. Regarding claims 32-35, claim 32 recites, "... and [sic: said] second semiconductor region has an impurity concentration higher..." (Fourth from last line)

c. Appropriate correction is required

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-3, 22, 24 (as interpreted above), 26, 27, 29-31, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP '974 (made of record in the Office Action of 6/20/02; paper #13) in view of Howard, Jr. '179 (previously cited) and Takahashi '872.

a. JP '974 discloses a Zener diode structure comprising[1] a type II (n-type) semiconductor substrate 1; a p-type (type-I) well region 2; a first, n-type semiconductor region 10, 11a formed in the well; a second, p-type semiconductor region 9 formed in the well at the bottom of the central portion of n-region 10. The peripheral n-portion 11a extends deeper and surrounds the central n-portion 10 (e.g., claim 3). The p-region 9 is more heavily doped (1e16)

[1]Applicant uses different terminology to reference a given region in various claim sets. The following rejection will use the terminology employed in claim 1 unless otherwise noted.

than the p-type well 2 (5e15) (page 3, lower right column) (e.g., claims 24, 26 and 27). A plurality of through holes extend through insulating layer(s) 3 and/or 13, with a first plurality of connection holes 7/6 extending therethrough to contact the n region 10, and a second plurality of connection holes 8/6 extending therethrough to contact the p well at a region peripherally exterior to the n region 9. Semiconductor regions 9 and 10 form a first pn junction. N-substrate 1 and p-well 2 form a second pn junction. As the Zener breakdown occurs between the first pn junction, producing a current Iz (FIG 2), the breakdown voltage of the second pn junction is greater than that of the first junction. Restated, JP '974 does not anticipate these claims because it teaches all of the limitations set forth therein except for the following two limitations.

b. JP '974 teaches the plurality of first connection holes contacting the shallow central portion 10 of the n-type semiconductor region 10/11a instead of the peripheral portion 11a, as set forth by claims 2 and 29. Howard '179 teaches buried Zener diode structures comprising a p-region 24 and an overlying n-region 32 forming the pn junction are formed in N well 16 on p substrate 10. The metalization pattern extend through the overlying insulation to contact a portion of the n region (C) at a peripheral region remote from the shallowest portion of n-cathode 32 for the purpose of preventing spikethrough. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the buried Zener diode structure of JP '974 by moving the cathode contact holes 8/6 peripherally outward so as to instead contact the deeper peripheral portion 11a for the purpose of preventing spikethrough as taught by Howard.

c. JP '974, setting forth a single Zener diode, does not appear to further teach a plurality of serially-connected Zener diodes as set forth in, for example, the last clause of claim 1. Takahashi '872 discloses the use of Zener diodes in a clamping circuit for a differential input circuit. The Zener diodes may be serially connected for changing the Zener voltages of the clamp circuit (e.g., FIGs 12 and 13 and col. 9-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to have employed the Zener diode of JP '974 in a circuit such as a clamp circuit comprising a plurality of such diodes that are serially connected for the purpose of changing the Zener voltage as taught by Takahashi '872.

5. Claims 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP '974/Howard '179 as applied to the claims above, and further in view of Villa et al. '387 (previously made of record in the last Office Action).

a. The combination of JP '974/Howard '179 teach all of the limitations set forth in these claims as explained above except for the further limitation of claim 32 that the Zener diode be formed within a second well that is nested inside of a first well; rather, the references show the Zener diode being formed in a single well (e.g., well 2 of JP '974).

b. See for example FIG 5 wherein Villa teaches a Zener diode structure wherein the cathode portion is comprised of a shallow N+ region and a surrounding peripheral N+ region of deeper diffusion with the cathode contact formed on the deeper peripheral region, thereby preventing spikethrough. The anode electrode contacts the p (type II) well that is nested within

an n (type I) well that is, in turn, formed on a p-type substrate. Villa does not anticipate the claims because it does not further disclose a more highly doped p semiconductor region formed within the p-well subjacent the central portion of the cathode.

c. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the Zener diode structure of JP '974/Howard that is formed in a p-well on an n-type substrate so as to instead be formed on a p-type substrate that is separated from the p-type well by a second, n-type well as taught by Villa depending only upon conventional considerations that were well known to the skilled artisan such as the specific circuitry with which the Zener diode is to be monolithically integrated, which in turn, may dictate whether the substrate chosen would specifically be n-type or p-type.

6. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP '974 in view of Howard, Jr. '179, Takahashi '872 and Villa et al. 387 as respectively applied to the claims above.

a. Claim 36 includes the limitations of both claim sets set forth and addressed above in the preceding two rejections of paragraph numbers 4 and 5. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified or included within the JP '974 reference all of these features for the reasons set forth above.

b. Claim 36 further sets forth that the two p (type-I), second well regions of the respective diodes are both formed in the same n (type-II), first well region. Regardless of whether the disclosure of Takahashi relating to the provision of serially-connected Zener diodes and the

associated schematic depictions of the figures are, themselves, sufficient to render this limitation obvious, Villa teaches that a plurality of components may be integrated by forming them within the same well region (e.g., the N well region of FIG 5) by the use of oppositely-doped isolation regions, as desired. It would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the plurality of serially-connected Zener diodes within a common well for the well-known purposes of reducing space requirements and thereby also improving device response by reducing the wiring resistance relative to if the Zener diodes were formed further apart in separate wells.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

a shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. William Baumeister

Patent Examiner, Art Unit 2815

April 5, 2003